EEE7032-Embedded Systems
Spring 2019
Syllabus

What you will learn

- How programs are translated into the machine language
  - And how the hardware executes them
- The hardware/software interface
- What determines program performance
  - And how it can be improved
- How hardware designers improve performance
- What is parallel processing

Your background should be

- Basic knowledge about microprocessors/ microcontrollers
  - Any kind of assembly would be helpful
- Knowledge about any of high level programming languages:
  - C#
  - C, C++
  - Java
  - …
- Knowledge about any of Hardware Description Languages (HDL):
  - VHDL
  - Verilog
  - SystemC
  - …

Course Website, TextBook, Lecture Hours

- Course web site:
  http://www.salihbayar.com/Marmara/EEE7032.php

- There is no need to buy any Text Book
  - But follow:
    - Computer Organization and Design MIPS Edition 5th Edition-The Hardware/Software Interface, David **Patterson** John **Hennessy**
    - Computer Organization and Design ARM Edition -The Hardware/Software Interface, David **Patterson** John **Hennessy**
    - Computer Organization and Design RISC-V Edition -The Hardware/Software Interface, David **Patterson** John **Hennessy**
- 3 hours of class every week (No LAB)
  - 3 hour lectures (lectured by the instructor)
    - 3 Lecture Hours: Monday, 09:30 – 12:20

Software Programs and Tools

- **MARS (MIPS Assembler and Runtime Simulator)**
  - An IDE for MIPS Assembly Language Programming
  - http://courses.missouristate.edu/KenVollmar/mars/

- **LOGISIM (An educational tool for designing and simulating digital logic circuits)**
  - Design circuits using an intuitive graphical interface
  - Watch the circuits be simulated as they are drawn
  - https://sourceforge.net/projects/circuit/

- **Any kind of IDE for high level programming languages (Assembler & Disassembler Design)**
  - **Codeblocks, DevC++:** C, C++
  - **Microsoft Visual Studio Community Edition:** C, C++, C#
  - **Eclipse:** Java, C++
  - **WEB & Mobile:** Django (Python), PHP, JavaScript, Jquery, Ruby, Java, Swift, Objective C (Of course HTML5 + CSS)

- **Hardware Design Platforms using HDL**
  - **ISE Design Suite (14.7 Currently and latest version; discontinued)**
    - https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools.html
  - **Vivado HL WebPACK Edition (2018.3 Currently)**
    - https://www.xilinx.com/support/download.html

Grading

- Project-1 (Midterm Grade 50%) 10%
- Project-2 (Midterm Grade 50%) 10%
- Academic Presentation 20%
- Project-3 10%
- Attendance (If your attendance<70%, you fail!)
  - You have to attend at least 10 weeks.
- Final Report 50% (Both final grade and average must be at least 65/100 for MS and 75/100 PhD students according to faculty rules, otherwise you fail the course)

Projects (Tentative)

- Project-1 (Midterm Grade 50%) 10%
- Project-2 (Midterm Grade 50%) 10%
- Academic Presentation 20%
- Project-3   10%
- Attendance (If your attendance<70%, you fail!)
  - You have to attend at least 10 weeks.
- Final Report 50% (Both final grade and average must be at least 65/100 for MS and 75/100 PhD students according to faculty rules, otherwise you fail the course)

- Project-1
  - Implementing any Deep Learning / Machine Learning / Data Mining / Image Processing Algorithm/ Security (Encryption/ Decryption) Algorithm using cores from https://opencores.org/ on FPGA
- Project-2
  - 32-bit Single Cycle MIPS/ ARMv8/ RISCV CPU Design and Implementation using Logisim or any HDL (Verilog/VHDL/SystemC/SystemVerilog)
- Academic Presentation
  - Presentation of a Conference/Journal paper or an advanced topic in Embedded Systems
- Project-3
  - Implementing any Parallelizable Deep Learning / Machine Learning / Data Mining / Image Processing Algorithm/ Security (Encryption/ Decryption) Algorithm as HW on FPGA

Course outline (Tentative)

WEEK-1 (04.02.2019) Syllabus & Introduction
WEEK-2 (11.02.2019) Sample Algorithms and Applications of Embedded Systems
WEEK-3 (18.02.2019) Introduction to the VHDL
WEEK-4 (25.02.2019) Basics of VHDL
WEEK-5 (04.03.2019) Advanced Topics in VHDL (Project-1 Assignment)
WEEK-6 (11.03.2019) Sample VHDL Codes Using Xilinx Vivado
WEEK-7 (18.03.2019) Instructions: Language of the Computer and MIPS
WEEK-8 (25.03.2019) ARM8 & RISC-V Instruction Set (Academic Paper Selection Deadline)
WEEK-9 (01.04.2019) The Processor: MIPS & ARM8 & RISC-V (Project-2 Assignment)
WEEK-10 (08.04.2019) MIDTERM BREAK
WEEK-11 (15.04.2019) Academic Presentations-1
WEEK-12 (22.04.2019) Academic Presentations-2 (Project-3 Assignment)
WEEK-13 (29.04.2019) Academic Presentations-3
WEEK-14 (06.05.2019) Academic Presentations-4
WEEK-15 (13.05.2019) Academic Presentations-5
WEEK-16 (20.05.2019) Academic Presentations-6
21.06.2019 -> Final Report Deadline